Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A semiconductor device comprising:

a bus master;

a bus interface that controls access to at least one semiconductor storage medium based on request for access to the at least one semiconductor storage medium from the bus master, the at least one semiconductor storage medium including a plurality of semiconductor storage media, the bus interface including a plurality of dedicated bus interfaces that each correspond to one of the plurality of semiconductor storage media; and

a clock-supply-control circuit that controls the presence of the supply of a clock to the bus interface based on access state information that indicates a state of access to the at least one semiconductor storage medium, the clock-supply-control circuit including a circuit, the circuit implementing at least one of control for stopping the supply of the clock to the bus interface if the circuit determines that access is not in execution, and control for supplying the clock to the bus interface if the circuit determines that access is in execution, based on the access state information;

the first dedicated bus interface block stopping to receive a clock signal a first predetermined time elapsed after an access of the first dedicated bus interface block to the first storage medium is completed,

the second dedicated bus interface block stopping to receive a clock signal a second predetermined time elapsed after an access of the second dedicated bus interface block to the first storage medium is completed.

2. (Previously Presented) The semiconductor device according to Claim 1,

the bus interface further including

a common bus interface that in common implements operation required for access control when access to any of the plurality of semiconductor storage media is in execution;

the plurality of dedicated bus interfaces each correspond to a certain one of the plurality of semiconductor storage media and that each implement operation required for access control only when access to the certain one of the plurality of semiconductor storage media is in execution; and

the clock-supply-control circuit detects any of the plurality of semiconductor storage media that is other than any of the plurality of semiconductor storage media that is to be accessed based on accessed-medium information indicating which semiconductor storage medium is to be accessed, and controls so as to stop the supply of the clock to any of the plurality of dedicated bus interfaces for the any of the plurality of semiconductor storage media that is other than the any of the plurality of semiconductor storage media that is to be accessed and supply the clock to any of the plurality of dedicated bus interfaces for the any of the plurality of semiconductor storage media that is to be accessed.

3. (Previously Presented) The semiconductor device according to Claim 1, the clock-supply-control circuit implementing a process to stop the supply of the clock to the bus interface after the completion of a valid signal output from the bus interface.

4. (Previously Presented) A semiconductor circuit that controls a presence of a supply of a clock to a bus interface controlling access to at least one semiconductor storage medium based on request for access to the at least one semiconductor storage medium from a bus master, comprising:

a control-signal generator that generates a clock-supply-control signal for the bus interface for instructing the presence of the supply of the clock to the given bus interface,

based on access state information that indicates a state of access to the at least one semiconductor storage medium; and

a control circuit that controls the presence of the supply of the clock generated from a clock generator to the given bus interface, based on the clock-supply-control signal for bus interface,

the control-signal generator disabling the clock-supply-control signal for bus interface if the access state information indicates that access is not in execution;

the control circuit including a circuit that controls so as to stop the supply of the clock generated from the clock generator to the bus interface if the clock-supply-control signal for the bus interface is disabled;

the at least one semiconductor storage medium including a plurality of semiconductor storage media; and

the bus interface including a plurality of dedicated bus interfaces that each correspond to one of the semiconductor storage media;

the first dedicated bus interface block stopping to receive a clock signal a first predetermined time elapsed after an access of the first dedicated bus interface block to the first storage medium is completed,

the second dedicated bus interface block stopping to receive a clock signal a second predetermined time elapsed after an access of the second dedicated bus interface block to the first storage medium is completed.

5. (Previously Presented) The semiconductor circuit according to Claim 4,

the bus interface further including

a common bus interface that in common implements operation required for access control when access to any of the semiconductor storage media is in execution;

the dedicated bus interfaces each implement operation required for access control only when access to the certain one of the semiconductor storage media is in execution;

the control-signal generator detects any of the semiconductor storage media that is other than any of the semiconductor storage media that is to be accessed based on accessed-medium information shown by the bus interface and indicating which semiconductor storage medium is to be accessed, so as to disable a clock-supply-control signal for dedicated bus interface to any of the dedicated bus interfaces for the any of the semiconductor storage media that is other than the any of the semiconductor storage media that is to be accessed; and

the control circuit includes a circuit that controls so as to stop the supply of the clock generated from the clock generator to the any of the dedicated bus interfaces for the any of the semiconductor storage media that is other than the any of the semiconductor storage media that is to be accessed if the clock-supply-control signal for dedicated bus interface is disabled.

6. (Original) The semiconductor circuit according to Claim 4, the control-signal generator disabling the clock-supply-control signal for dedicated bus interface after the completion of a valid signal from the bus interface.

7. (Original) Electronic equipment, comprising:

a semiconductor device that includes the semiconductor device according to Claim 1;

an input device that receives input information; and

an output device that outputs a result processed by an information-processing device based on the input information.

8. (Original) Electronic equipment, comprising:

a semiconductor device that includes the semiconductor circuit according to Claim 4;

an input device that receives input information; and

an output device that outputs a result processed by an information-processing device based on the input information.

9. (Previously Presented) A method of controlling clock-supply that controls the presence of a supply of a clock to a bus interface of a semiconductor device, comprising:

generating a clock-supply-control signal for the bus interface for instructing the presence of the supply of the clock to a given bus interface, based on access state information that indicates a state of access to at least one semiconductor storage medium; and

controlling the presence of the supply of the clock generated from a clock generator to the given bus interface, based on the clock-supply-control signal for bus interface,

the clock-supply-control signal for bus interface being disabled if the access state information indicates that access is not in execution;

control to stop the supply of the clock generated from the clock generator to the bus interface block being implemented if the clock-supply-control signal for bus interface is disabled,

the at least one semiconductor storage medium including a plurality of semiconductor storage media, and

the bus interface including a plurality of dedicated bus interfaces that each correspond to one of the semiconductor storage media;

the first dedicated bus interface block stopping to receive a clock signal a first predetermined time elapsed after an access of the first dedicated bus interface block to the first storage medium is completed,

the second dedicated bus interface block stopping to receive a clock signal a second predetermined time elapsed after an access of the second dedicated bus interface block to the first storage medium is completed.

10. (Previously Presented) The method of controlling clock-supply according to Claim 9, the bus interface further including:

a common bus interface that in common implements operation required for access control when access to any of the semiconductor storage media is in execution;

the dedicated bus interfaces each implement operation required for access control only when access to a certain one of the semiconductor storage media is in execution;

any of the semiconductor storage media that is other than any of the semiconductor storage media that is to be accessed is detected based on accessed-medium information shown by the bus interface and indicating which semiconductor storage medium is to be accessed, and a clock-supply-control signal for dedicated bus interface to any of the dedicated bus interfaces for the any of the semiconductor storage media that is other than the any of the semiconductor storage media that is to be accessed is disabled; and

control is implemented so that the supply of the clock generated from the clock generator to the any of the dedicated bus interfaces for the any of the semiconductor storage media that is other than the any of the semiconductor storage media that is to be accessed is stopped if the clock-supply-control signal for dedicated bus interface is disabled.

11. (Original) The method of controlling clock-supply according to Claim 9, the clock-supply-control signal for the dedicated bus interface being disabled after the completion of a valid signal from the bus interface.

12. (Previously Presented) The semiconductor device according to Claim 1,

the bus interface outputting a BUSY signal to the clock-supply-control circuit,

the BUSY signal indicating the access of the bus interface being in execution, and

the clock-supply-control circuit implementing a control for stopping the supply of the clock to the bus interface at least one clock cycle elapsed after the access completion indicated by the BUSY signal.

13. (Currently Amended) A semiconductor device, comprising:

a bus master; and

a bus interface that includes a plurality of ~~first~~ dedicated bus interface blocks, each of the ~~plurality of the~~ plurality of ~~first~~ dedicated bus interface blocks accesses ~~to~~ one storage medium of a plurality of storage media,

the semiconductor device being configured such that:

a first ~~first~~ dedicated bus interface block of the plurality of ~~first~~ dedicated bus interface blocks receives a clock signal during at least a part of a first period in which the first ~~first~~ dedicated bus interface block accesses ~~to~~ a first storage medium of the plurality of storage media,

the first ~~first~~ dedicated bus interface block does not receive a clock signal during at least a part of a second period in which the first ~~first~~ dedicated bus interface block does not access ~~to~~ the first storage medium,

a second ~~first~~ dedicated bus interface block of the plurality of first bus interface blocks receives a clock signal during at least a part of a third period in which the second ~~first~~ dedicated bus interface block accesses ~~to~~ a second storage medium of the plurality of storage media; and

the second ~~first~~ dedicated bus interface block does not receive a clock signal during at least a part of a fourth period in which the second ~~first~~ dedicated bus interface block does not access ~~to~~ the second storage medium.

14. (Currently Amended) The semiconductor device according to Claim 1, the bus interface further including a second bus interface block that accesses ~~to~~ at least one of the plurality of storage media designated by the bus master.

15. (Previously Presented) The semiconductor device according to Claim 3, a length of the predetermined time being longer than one clock cycle.